9. Troubleshooting

Contents

Troubleshooting

The troubleshooting instructions include the following items:

1 Phone is totally dead

2 Flash programming does not work

3 Power does not stay on or phone is jammed

4 "Contact Service" is displayed

5 Phone does not register to the network or phone does not make a call

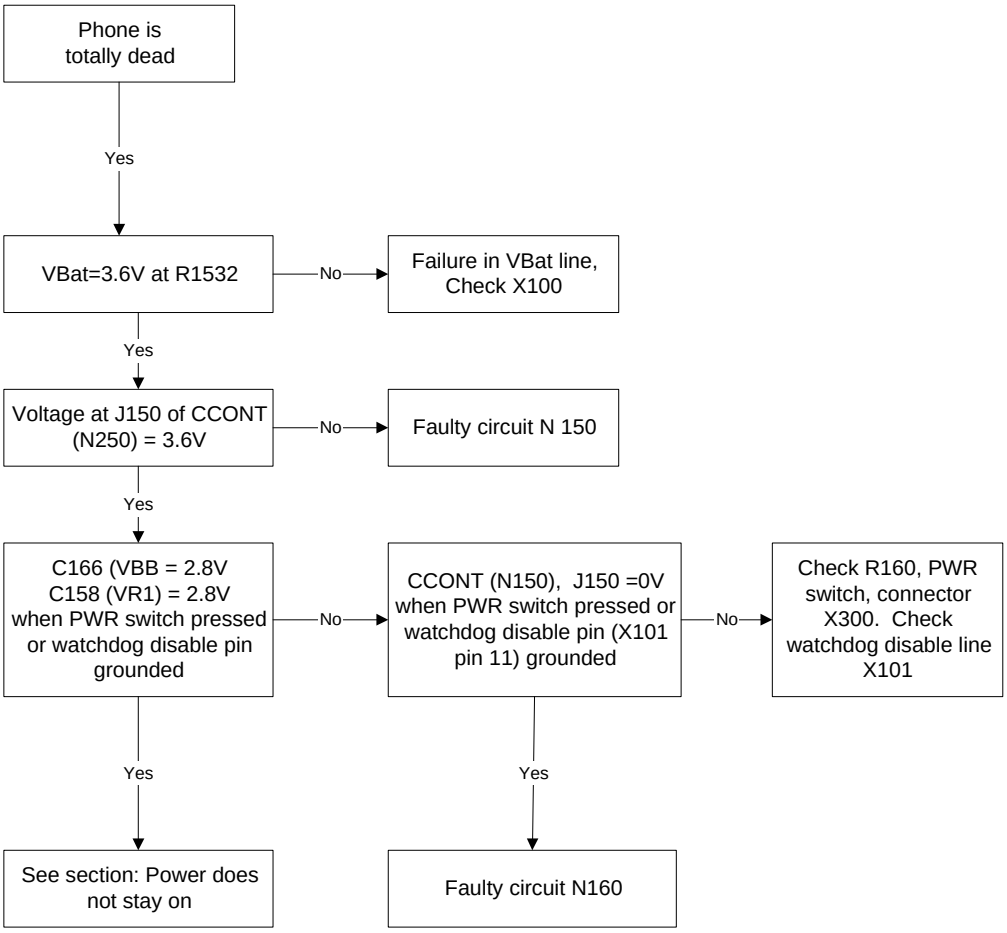
6 Audio fault

7 Charging fault

If any of these problems is encountered, the first recommendation is to carry out a thorough visual inspection of the module. In particular, observe if there is any mechanical damage and that the solder joints are OK.

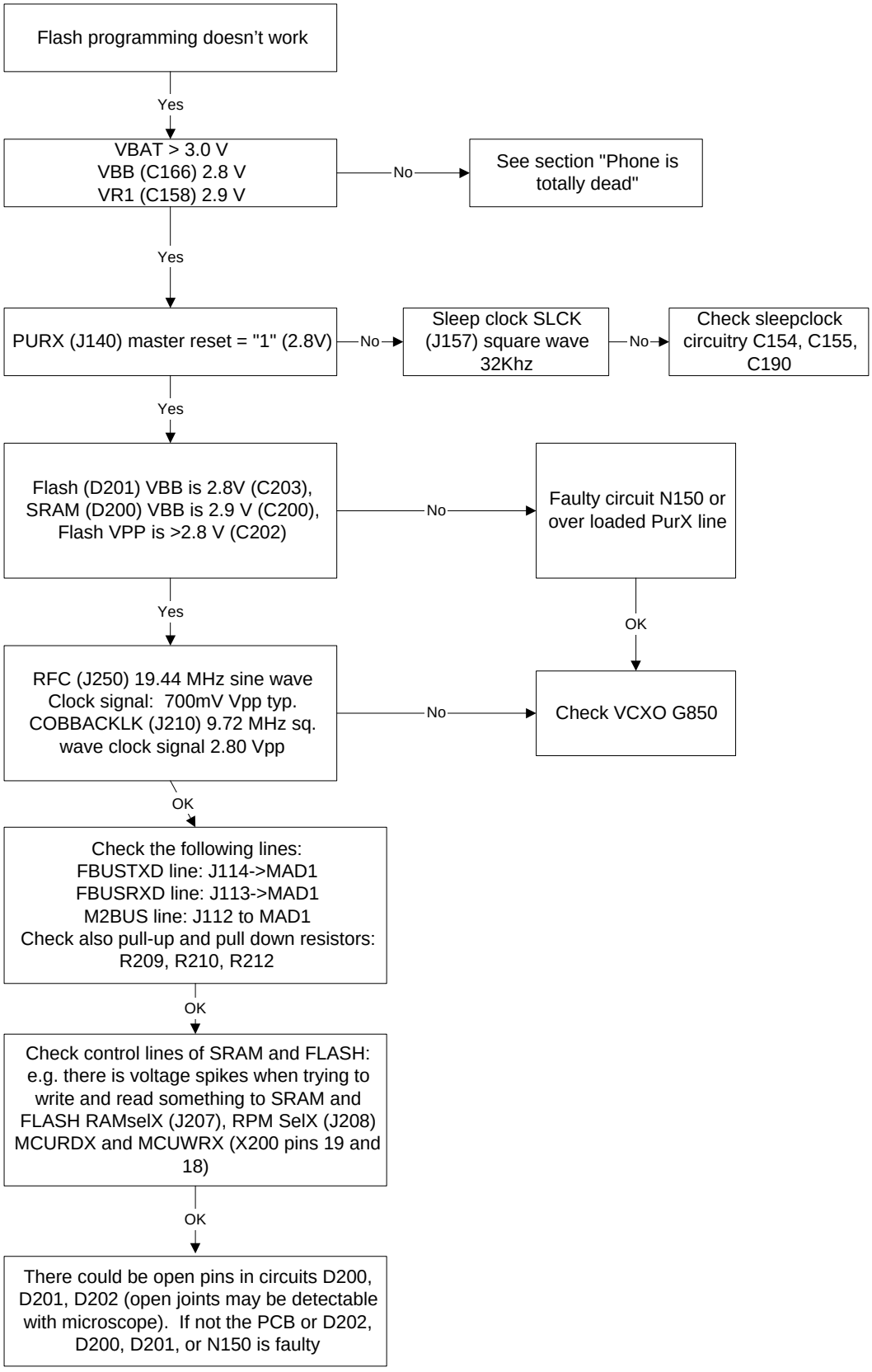
Phone is Totally Dead

The phone doesn't take current at all when the power switch is pressed or when the watchdog disable pin (X101 pin 11 or J150) is grounded. Used battery voltage must be higher than 3.0V. Otherwise, the hardware of CCONT (N150) prevents totally switching power on. Here, the VBAT is set to 3.6.



Flash Programming Doesn't Work

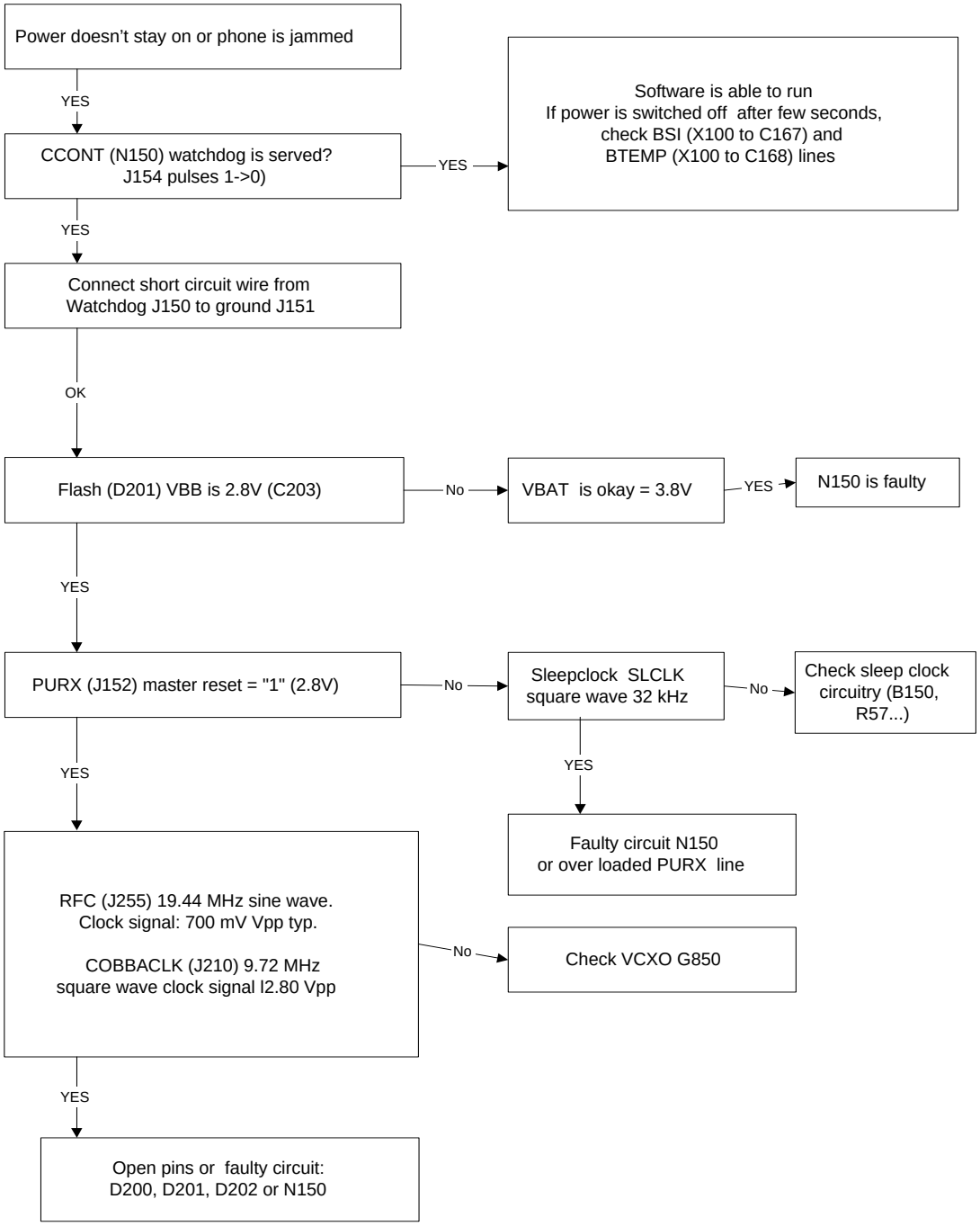
The flash programming is carried out via the pads accessible from the back of the phone(using service accessories).



Phone Doesn't Stay on or Phone is Jammed

If this fault occurs *after* flash programming, there are likely open pins in ICs. The solder joints of ICs: MAD1 (D202), Flash (D201), and SRAM (D200) should be checked to the extent possible (by microscope from the side of the PWB). Lightly press components while switching the power on.

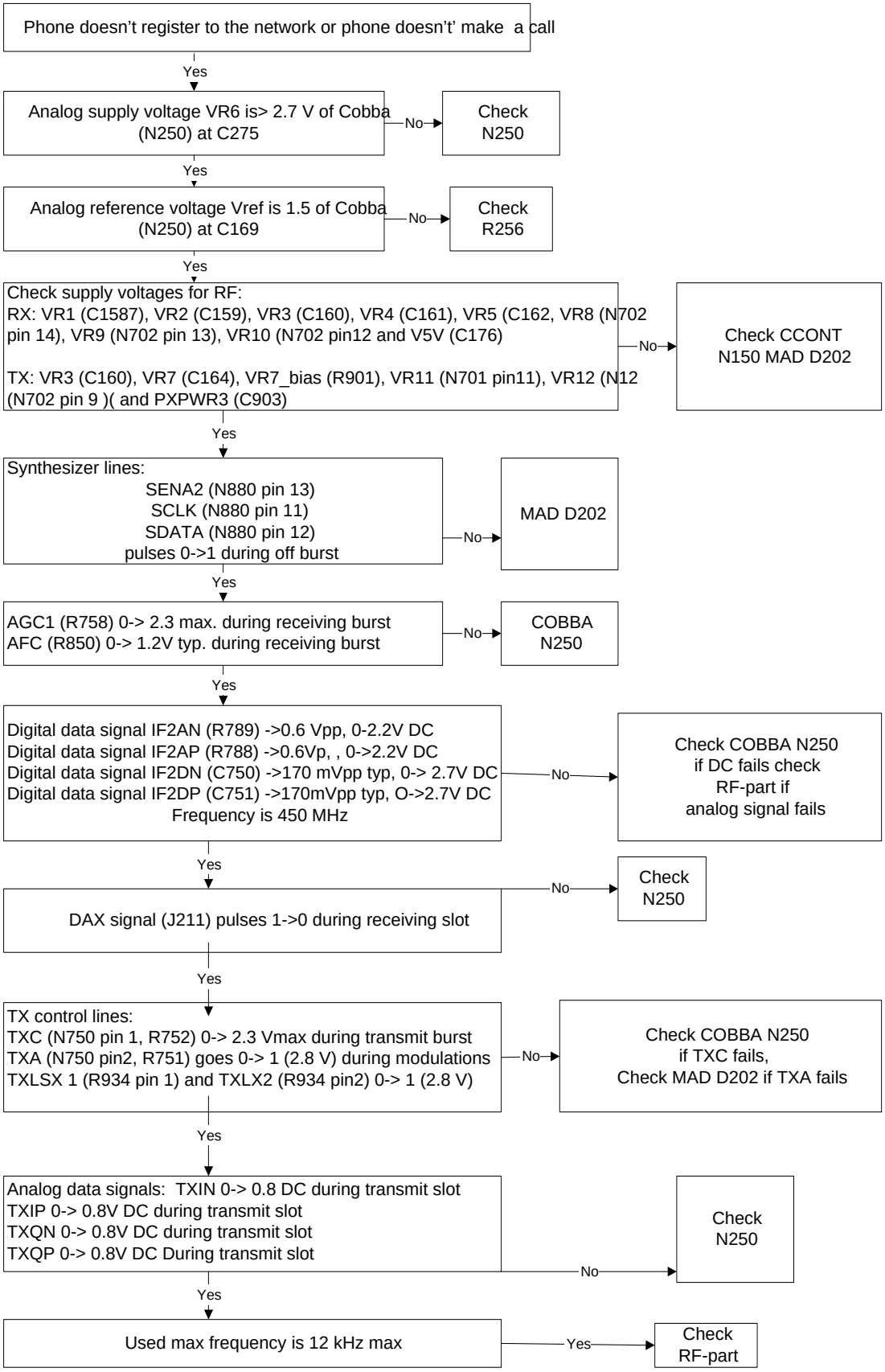
Normally, the power will be switched off by CCONT (N150) after 32 seconds. If the CCONT watchdog cannot be served by software, the watchdog updating may be viewed by oscilloscope at J154 (DataselX) of CCONT. Normally, there is a short pulse from "1"-> 0 every 8 seconds. The power-off function of CCONT can be prevented by connecting a short circuit wire from WDDISX (CCONT E4 J150) to ground (J151).



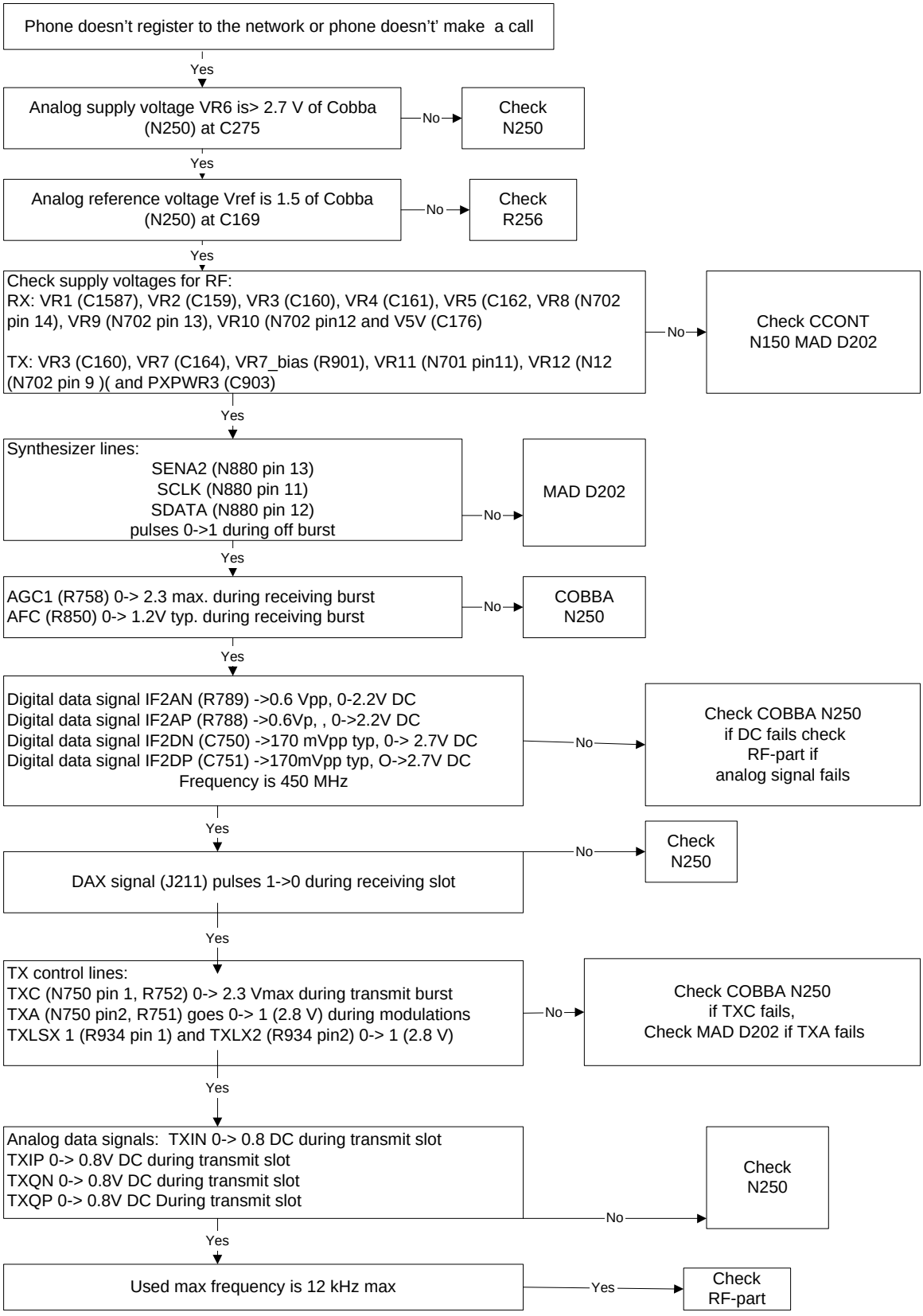
Phone Doesn't Register to the Network or Phone Doesn't Make a Call

If the phone doesn't register to the network or the phone doesn't make a call, the likely items to troubleshoot are the baseband or the RF. The phone may be set to "Wanted" mode by WinTesla service software in order to determine if the fault is located in the RF or the baseband (RF interface measurements).

The control lines for RF are supplied by both the System Asic (MAD D202) and the RFI (Cobba N250). MAD handles the digital control lines and Cobba handles analog control lines.



Charging Failure



RF Troubleshooting

Introduction

Measurements are done using a spectrum analyzer and a high-frequency probe (local and reference frequencies and RF-power levels in intermediate stages of TX/RX-chains). An oscilloscope is used to measure DC-voltages and low-frequency signals. A multimeter also is a useful measurement instrument for fault-finding.

An external RF connector is assembled only for R&D purposes — calibration panels for FLALI improving reliability of the measurement results; it should be in use whenever possible. Soldering pads for this connector will later be removed from the layout; therefore, a connector to the antenna pad needs to be soldered manually.

The RF section is mainly built around EROTUS-IC (N700). The RF block has separate external filters, UHF synthesizers, Power Amplifiers, TX Driver amplifiers, LNA/mixer, and upconverter circuit for both frequency bands. In TDMA 1900 mode, an RF regulator IC is provided to supply voltage for RF parts.

To simplify troubleshooting, this RF troubleshooting section is divided into three sections: Receiver, Transmitter, and Synthesizer blocks. Tolerances are specified for critical signals/voltages.

Before changing ASICs or components, check the following items:

1. Soldering and connections of ASICs pins
2. Supply voltages and control signals
3. Signals from synthesizers are coming to ASICs (prevents unnecessary changing of ASICs).

Note that the grounding of the Power Amplifier-IC is directly underneath **???what**, which makes it difficult to check. The PA is ESD sensitive. ESD precautions must be used when dealing with the PA-IC (ground straps and ESD soldering irons). The PAs also are moisture-sensitive components, making it important to follow additional information about component handling.

There are many discrete components (resistors, inductors, and capacitors) that may have troubleshooting done simply by checking that the component is soldered or that the component is not missing from the PWB.

Abbreviations used

BB	Baseband
f	Frequency of signal (measured with spectrum analyzer)
IF	Intermediate Frequency
LO	Local Oscillator
P	Power of signal in decibels compared to a milliwatt (dBm) (measured with spectrum analyzer)
PA	Power Amplifier
PWB	Printed Wiring Board
PLL	Phase Locked Loop
RF	Radio Frequency
RX	Receiver
T	Time (between pulses)
TX	Transmitter
UHF	Ultra High Frequency
V	Voltage of signal (measured with oscilloscope)
VCO	Voltage controlled oscillator
VHF	Very High Frequency
AF	Audio Frequency

Interface signals between RF and BB/DSP

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Function
VBAT	Battery	RF	Voltage	3.1	3.6	5.3	V	Supply voltage for RF and regulators
VREF	CCONT	EROTUS	Voltage	1.478	1.500	1.523	V	Reference voltage for EROTUS
RFTEMP	RF	CCONT	Voltage	0 HOT	1.4 ROOM TEMP	2.7 COLD	V	RF temperature sensor 47k NTC to GND
AFC	COBBA_D	VCTCXO	Voltage	0.05	1.1	2.25	V	Automatic frequency control

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Function
AGC1	Cobba_D	EROTUS	Voltage	0.5		1.4	V	Gain control for EROTUS RX AGC
AGC2	MAD	RX LNA	Voltage	0		2.85	V	LNA Gain switch "1" min 2.0V "0" max 0.7V
PD1	EROTUS	VHF VCO	Voltage	0 1.0 2.8	 1.5 3.3	4.0 2.0 3.8	V V V	VCO control voltage 322.38MHz 392.46MHz
PD2	EROTUS	1GHz UHF VCO	Voltage	1.3		3.5	V	1 GHz
MODE	MAD	1Ghz PA bias switch	Voltage	0		2.85	V	"0" AMPS "1" TDMA
IF2AP/ IF2AN	EROTUS	COBBA_D	Voltage/ Frequency		0.6/450		Vpp/ kHz	Differential limiter output to DEMO-FM demodulator
SENA1	MAD	EROTUS	Logic high "1"	2.0		2.85	V	1 GHz PLL enable
			Logic low "0"	0		0.8	V	
SDATA	MAD	EROTUS	Logic high "1"	2.0		2.85	V	Synthesizer data
			Logic low "0"	0		0.8	V	
SCLK	MAD	EROTUS	Logic high "1"	2.0		2.85	V	Synthesizer clock
			Logic low "0"	0		0.8	V	
RFC	EROTUS	COBBA_D	Voltage/ Frequency	0.2	0.4/ 19.44	1.0	Vpp/ MHz	Clock signal for logic circuits
RFCEN	MAD	CCONT/ PENTA regulator	Voltage	0		2.85	V	"1" min 2.0V "0" max 0.4V
RSSI	EROTUS	CCONT/ COBBA_D	Output level	0.1		1.5	V	Analog mode field strength indicator

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Function
TXIP/TXIN	COBBA	EROTUS	Differential voltage swing (static)	1.022	1.1	1.18	Vpp	Differential in-phase TX baseband signal for RF modulator
			Single-ended output level	0.760	0.8	0.84	V	
TXQP/ TXQN	COBBA	EROTUS	Same as TXIP/TXIN					Differential quadrature phase TX baseband signal for RF modulator
TXP1	MAD	CCONT	Logic high "1"	2.0			V	1 GHz transmitter enable
			Logic low "0"			0.5	V	VR7 ON/OFF
TXC	COBBA	EROTUS	Number of bits	10			bits	Transmitter power control (ramps & power levels)
			Output voltage swing	2.09	2.15	2.21	V	
			Minimum code output level	0.12	0.15	0.18	V	
			Maximum code output level	2.27	2.3	2.33	V	
TXF	EROTUS	MAD	Voltage	0		2.85	V	False transmission indicator, function controlled via EROTUS register
TXP2	MAD	PENTA regulator	Logic high "1"	2.0			V	2 GHz transmitter enable
			Logic low "0"			0.5	V	VR11 ON/OFF

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Function
TXA	MAD	EROTUS	Logic high "1"	2.5			V	PWR control loop during TX burst (slow mode)
			Logic low "0"			0.2	V	PWR control loop during up/down (fast mode)
TXLX1	MAD	TX 800	Logic high "1"	2.1		2.85	V	Low power level mode for power detector
			Logic low "0"	1		0.6	V	High power level mode for power detector
SENA2	MAD	2 GHz UHF PLL	Logic high "1"	2.0		2.85	V	2 GHz PLL enable
			Logic low "0"	0		0.8	V	
RXPWR1	MAD	CCONT	Logic high "1"	2.0			V	VR4 ON
			Logic low "0"	0		0.8	V	VR4 OFF
RXPWR2	MAD	PENTA	Logic high "1"	2.0			V	VR8 ON, 1GHz frontend
			Logic low "0"	0		0.8	V	VR8 OFF
RXPWR3	MAD	PENTA	Logic high "1"	2.0			V	VR9 ON 2GHz frontend
			Logic low "0"	0		0.8	V	VR9 OFF
SPWR1	COBBA_D	CCONT	Logic high "1"	2.0			V	VR2 ON, 1GHz UHF
			Logic low "0"	0		0.5	V	VR2OFF
SPWR 2	COBBA_D	CCONT	Logic high "1"	2.0			V	VR3 ON, VHF ON/OFF
			Logic low "0"	0		0.5	V	VR3 OFF

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Function
SPWR3	COBBA_D	PENTA	Logic high "1"	2.0			V	VR10 ON, 2 GHz UHF
			Logic low "0"	0		0.5	V	VR10 OFF
TXPWR1	MAD	CCONT	Logic high "1"	2.0			V	VR5 ON, TX PWR control enable
			Logic low "0"	0		0.5	V	VR5 OFF
TXWR2	MAD	PENTA	Logic high "1"	2.0			V	VR12 ON TDMA 1900 TX-upconverter enable
			Logic low "0"	0		0.5	V	VR12 OFF
TXWR3	MAD	TDMA800 TX-upconverter	Logic high "1"	2.0			V	AMPS & TDMA 800 TX-upconverter enable
			Logic low "0"	0		0.5	V	TX-UC disable
VR1	CCONT	RF	Voltage	2.7	2.8	2.85	V	Supply for VCTCXO, EROTUS VHF prescaler and bias and 2GHz PLL
VR2	CCONT	RF	Voltage	2.7	2.8	2.85	V	Supply voltage for 1GHz UHF VCO and prescaler
VR3	CCONT	RF	Voltage	2.7	2.8	2.85	V	Supply voltage for VHF VCO, LO buffer, 1GHz TX-mixer and power detector
VR4	CCONT	RF	Voltage	2.7	2.8	2.85	V	Supply voltage for EROTUS TX modulator and TX PWR control circuits

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Function
VR5	CCONT	RF	Voltage	2.7	2.8	2.85	V	Supply voltage for EROTUS TX modulator and TX PWR control circuits
VR6	CCONT	RF	Voltage	2.7	2.8	2.85	V	Supply voltage for EROTUS digital parts and COBBA_D analog supply
VR7	CCONT	RF	Voltage	2.7	2.85	2.9	V	TX800 PA bias and driver amplifier supply voltage
VR7_bias	CCONT	RF	Voltage	2.7	2.85	2.9	V	TX800 PA bias switching voltage "0" = AMPS "1" = TDMA
V5V	CCONT	EROTUS	Voltage	4.8	5.0	5.2	V	EROTUS and 2GHz PLL charge pump

Receiver

General Instructions for RX Troubleshooting

Start the WinTesla software and use it to start the desired RX mode of the mobile phone. The troubleshooting flowchart is divided into three steps: general checking, local checking, and RX-chain checking. Before changing ASICs or filters, check all solderings and observe if any components are missing.

If any RX filters and/or ASICs are changed, AGC tunings must be made.

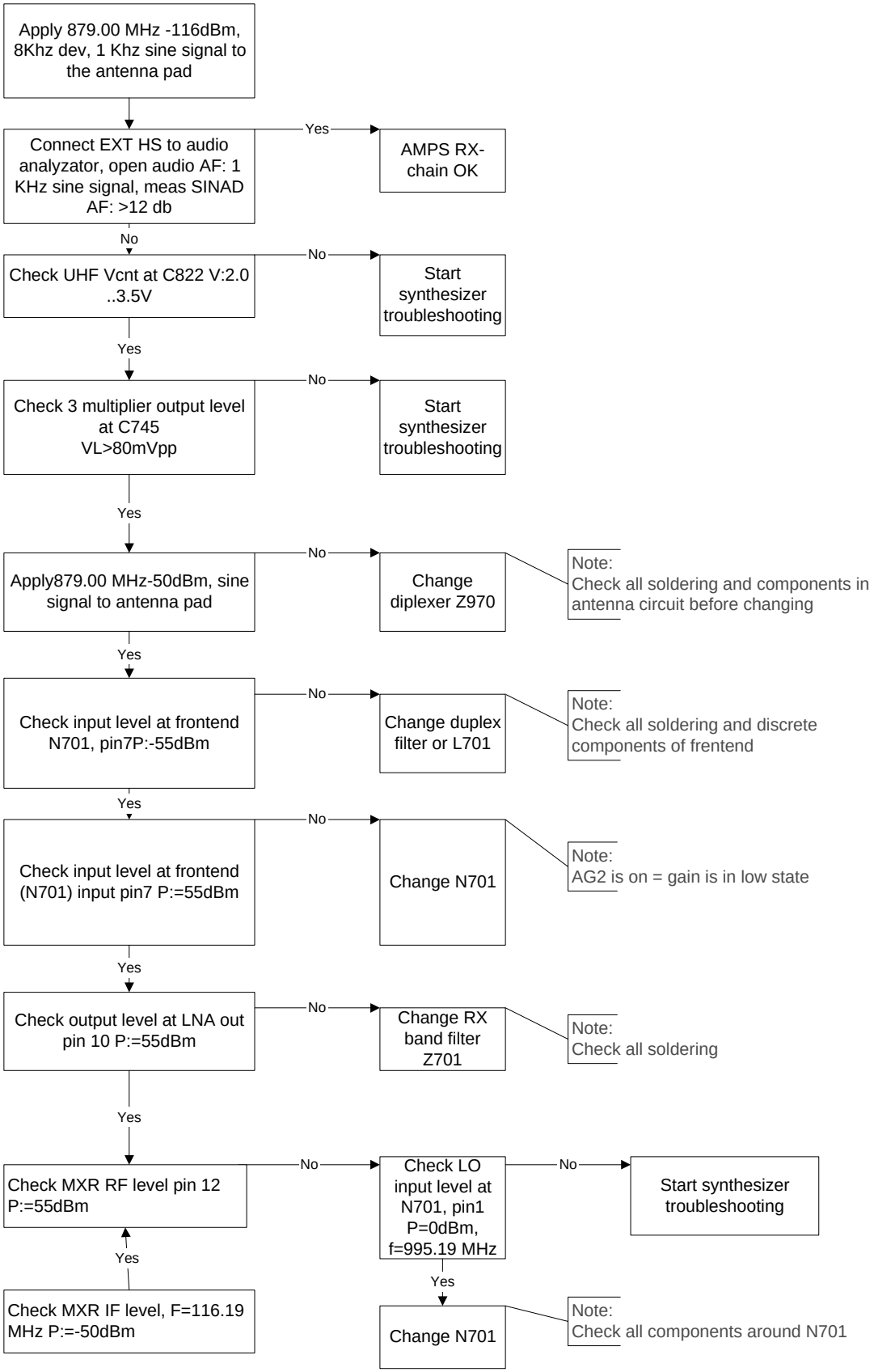
Connect the desired channel frequency and level to the antenna interface.

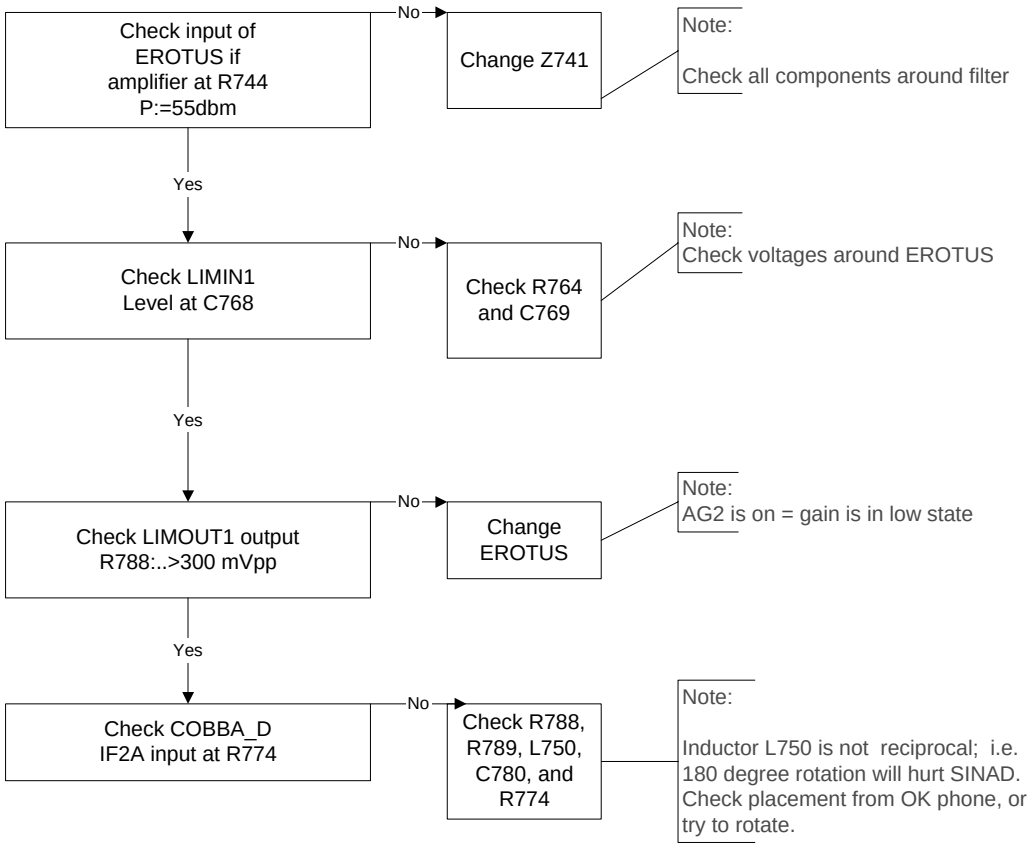
Path of the received signal

Block-level description of the receiver:
Antenna
Diplexer
Duplexer
Low-noise Amplifier (LNA)

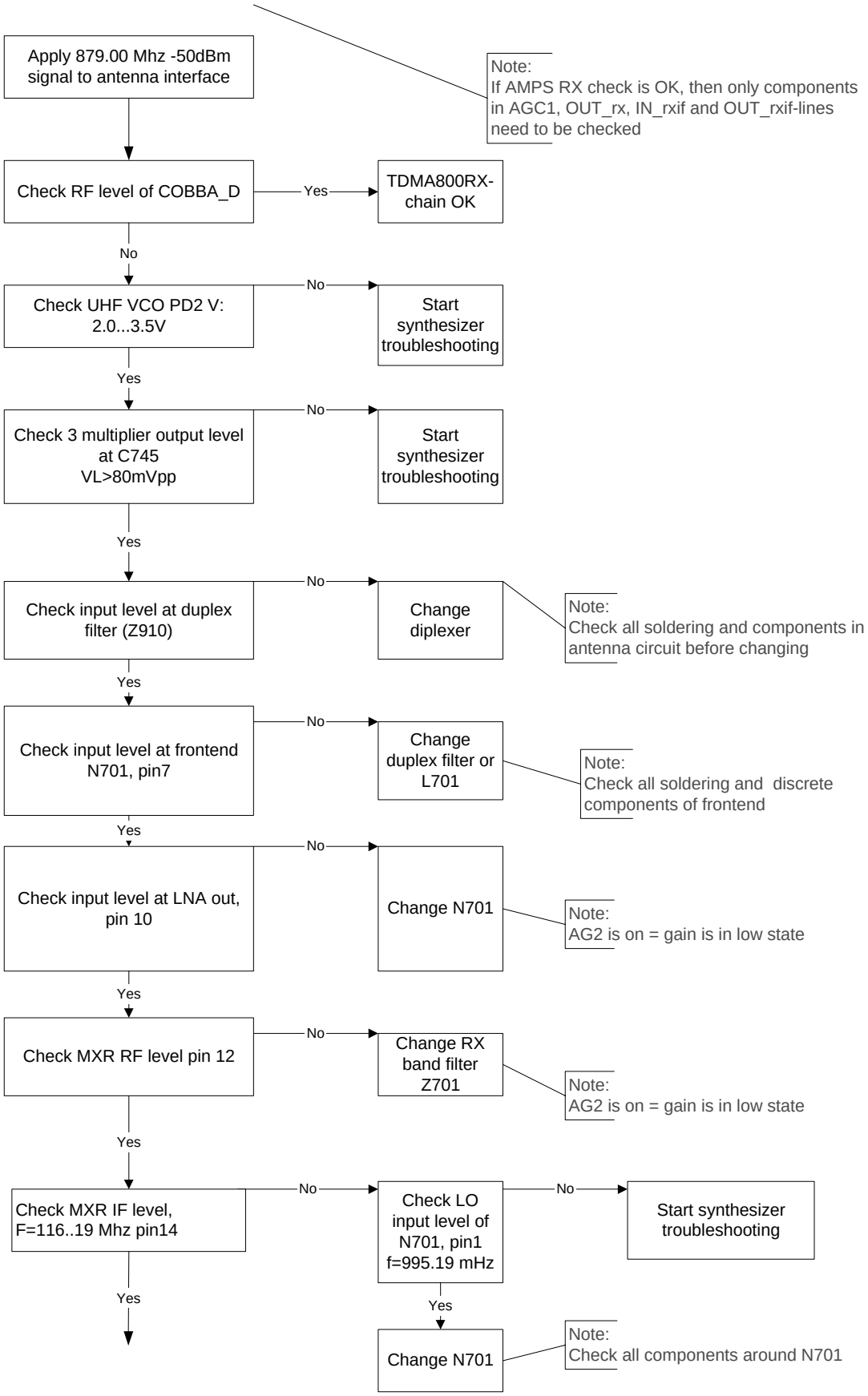
RX filter
First mixer
116.19 MHz filter
IF amplifier
AGC/buffer
second mixer
450 kHz filters
buffer/limiter
baseband (FM-detector)

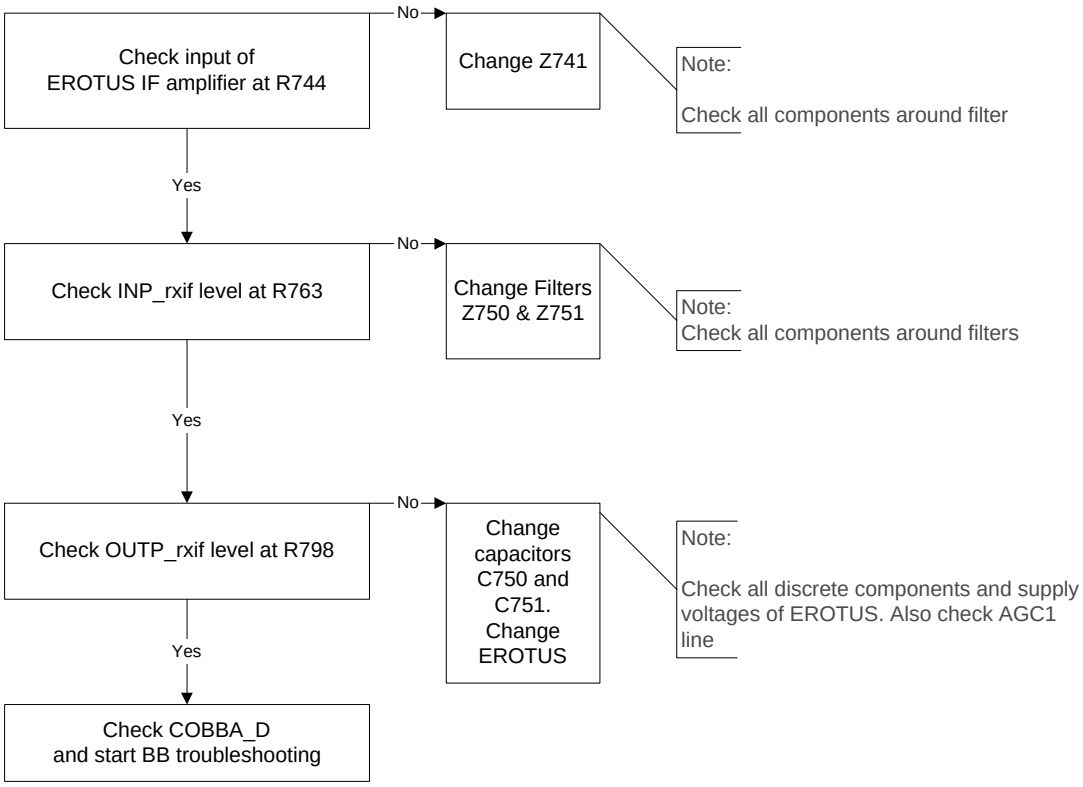
AMPS RX



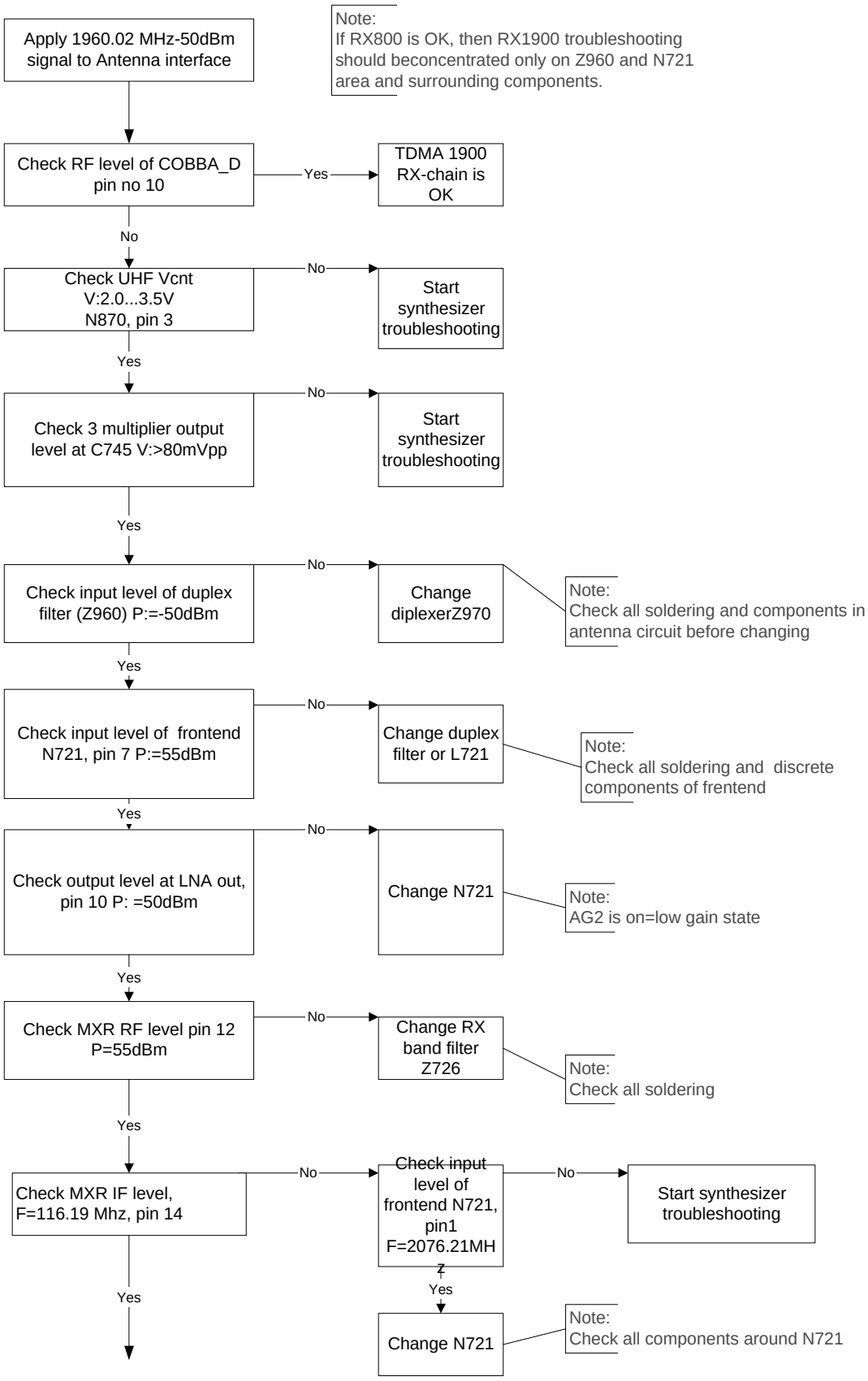


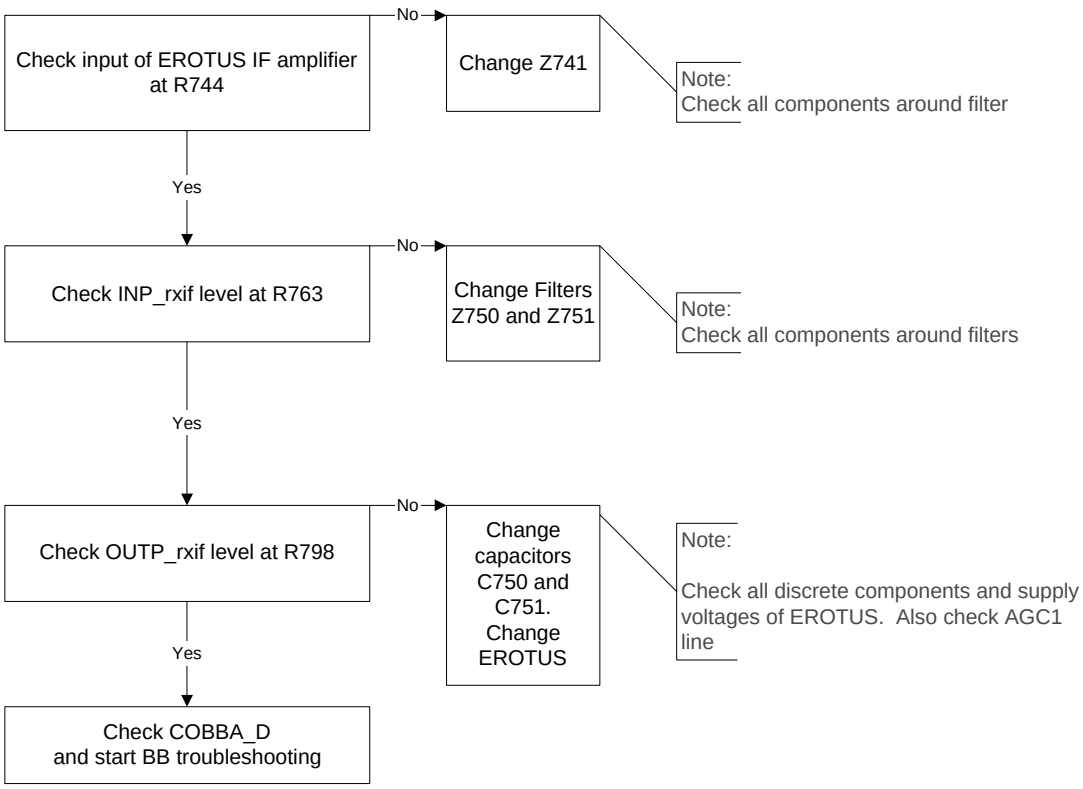
TDMA RX800





TDMA 1900RX





Transmitter

General Instructions for TX Troubleshooting

Always use the RF cable connected from antenna interface to analyzer through an attenuator. This is important to protect analyzer against excessive RF power and to stop unwanted RF power leak to the cellular frequencies.

Start the WinTesla software and select TX mode from Testing (AMPS, DAMPS, or TDMA 1900). It is useful to select mid-channel (383 for AMPS/DAMPS or 1000 for TDMA 1900) and power level 2. Select random data for digital mode of operation.

One of the basic tests monitors current when the transmitter is on. If current consumption does not change when the transmitter is set on, the fault is in the PA area.

Nominal current consumptions on power level 2 in mid-channel:

AMPS:	550-750 mA
TDMA800:	300-350 mA
TDMA1900:	350-400 mA

Note that if pressing the PA package more tightly to the PWB has an effect on current consumption, the fault is in the PA. In the case of a faulty PA, the replacement should be

done only under correct ESD precautions, using a hot air gun set to 10m/s and 300 degrees Centigrade. The new PA must be taken from a vacuum package and the heating process should be completed in less than 30 seconds. Note that the ground slug of the package must be properly soldered and excessive solder material, if any, has to be removed.

If any components in the TX chain are replaced, the power level tunings have to be checked and retuned.

Tuning targets are shown in the tables that follow.

Set power supply voltage.

Connect pulse power meter or spectrum analyzer. Use attenuator, if needed.

Set settings for spectrum analyzer in power level tuning:

Set span 0 Hz
Set Ref LVL 30 dB
Set Ref LVL offset and -> Attenuation to Antenna Pad
Set RBW and VBW 300 kHz
Set sweep time 50 ms
Set TRIG: SWEEP CONT, VIDEO -10 dBm
Set marker at middle of slot
Check that spectrum analyzer frequency is correct.

Set settings for pulse power meter:

Do calibration if needed
Set correct frequency
Set Ref LVL offset -> Attenuation to Antenna Pad
Set correct duty cycle, 33.3% in digital mode and 100% at analog mode
Select Tuning -> Using WinTesla Select Tuning -> TX power -> LowBand/High/ Band -> EEPROM values

All four tuning channels must be tuned. Repeat tuning for A, B, C, and D tuning channels. Tuning channel change read old tuning values from phone's EEPROM.

Adjust power level by clicking the **+** and **–** buttons, power level change is done by the **up** and **down** keyboard keys.

Tune power levels, which are shown by "# for calculate".

Press the **Calculate** button to calculate other power levels.

Check tuning; do fine tuning, if needed.

Once all TX tuning channels are correct, press the **Save** button.

Tuning is done if both analog mode and 800 MHz and 1900 MHz digital modes are tuned.

Difference between measured TX power from Test Pad of panel and Antenna Pad must be taken care so that measurements from Antenna Pad give the correct results.

Table 1: 800 MHz Analog TX Output Power

Power level	RF power at ext. Antenna Pad	Tuning target tolerance	Testing limits
2	24.8	=/- 0.1	0.5 /- 1dB
			24.3 / 25.8dBm

Table 2: 800 MHz Digital TX Output Power

Power level	RF power at ext. Antenna Pad	Tuning target tolerance	Testing limits
2	26.8 dBm	+/- 0.1 dB	0.5/- 1.0 dB
			27.3 - 25.8 dBm
3	23.5 dBm	+/- 1 dB	+/- 2.0 dB
4	20.0 dBm	+/- 1 dB	+/- 2.0 dB
5	16.0 dBm	+/- 1 dB	+/- 2.0 dB
6	12.0 dBm	+/- 1 dB	+/- 2.0 dB
7	8.0 dBm	+/- 1 dB	+/- 2.0 dB
8	4.0 dBm	+/- 1 dB	+/- 2.0 dB
9	-0.0 dBm	+/- 1 dB	+/- 2.0 dB
10	-4.0 dBm	+/- 1 dB	+/- 2.0 dB

Check that power level PL2 TXC DAC value is within the allowed range: +50 ... 300.

Table 3: TDMA 1900 TX Output Power

Power level	RF power at ext. Antenna Pad	Tuning target tolerance	Testing limits
2	25.9 dBm	+/- 0.1 dB	+0.5 ... - 1.0 dB
			26.4 - 24.9 dBm
3	23.0 dBm	+/- 1 dB	+/- 2.0 dB
4	20.0 dBm	+/- 1 dB	+/- 2.0 dB
5	16.0 dBm	+/- 1 dB	+/- 2.0 dB
6	12.0 dBm	+/- 1 dB	+/- 2.0 dB

Power level	RF power at ext. Antenna Pad	Tuning target tolerance	Testing limits
7	8.0 dBm	+/- 1 dB	+/- 2.0 dB
8	4.0 dBm	+/- 1 dB	+/- 2.0 dB
9	0.0 dBm	+/- 1 dB	+/- 2.0 dB
10	-4.0 dBm	+/- 1 dB	+/- 2.0 dB

Check that power level PL2 TXC DAC value is within the allowed range: +0 ... +250.

Path of the Transmitted Signal

AMPS/DAMPS

Cobba TX I/Q DAC - I/Q-modulator - gain step amplifier - linear gain control amplifier - IF BPF - Upconverter - TX Driver amplifier - BPF-P)ower Amplifier - Directional Coupler - Duplexer - Diplexer - Antenna.

TDMA 1900D

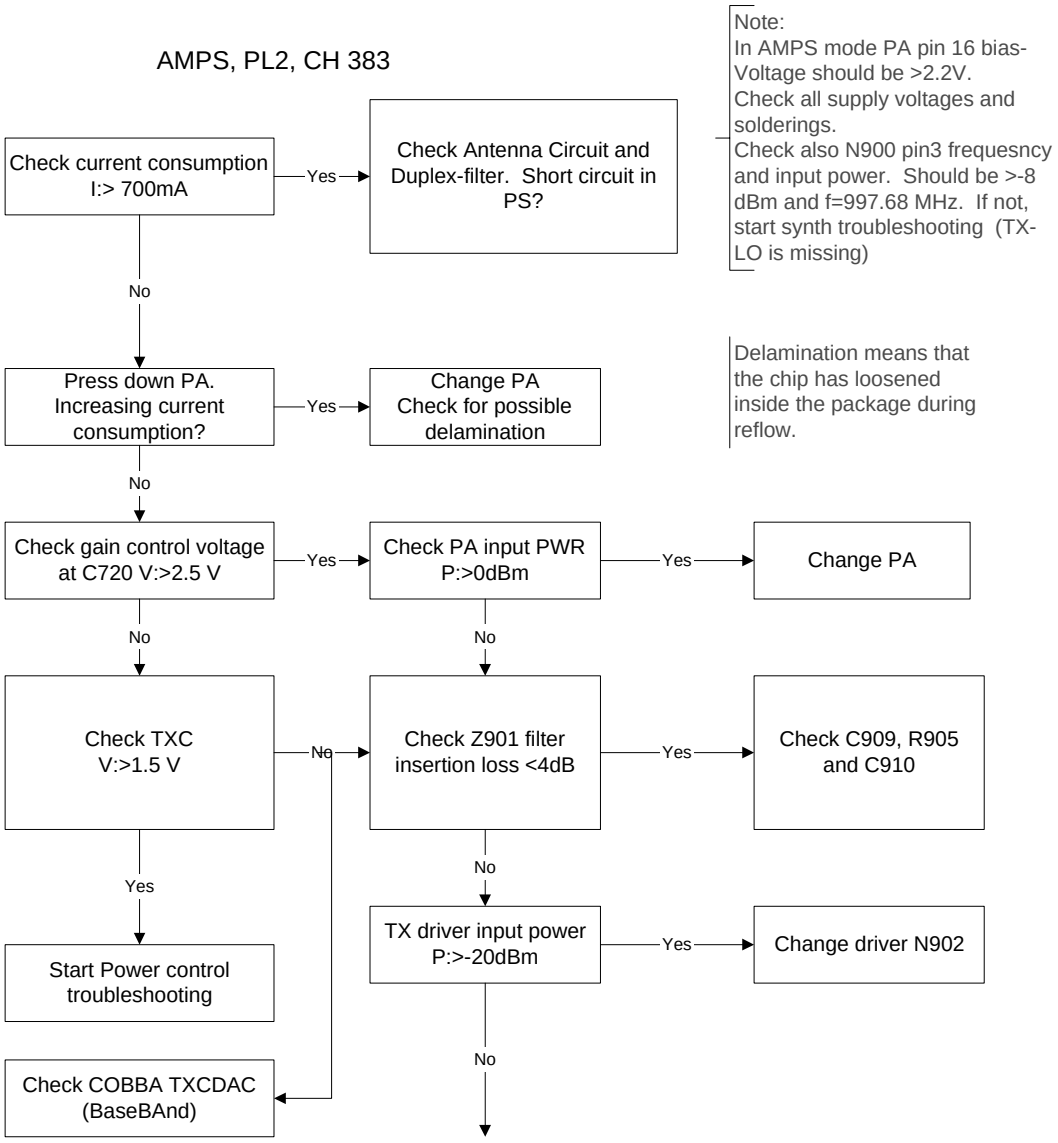
Cobba TX I/Q DAC - I/Q-modulator - gain step amplifier - linear gain control amplifier - IF BPF - Upconverter - BPF - TX Driver amplifier - BPF - Power Amplifier - Directional Coupler - Duplexer - Diplexer - Antenna

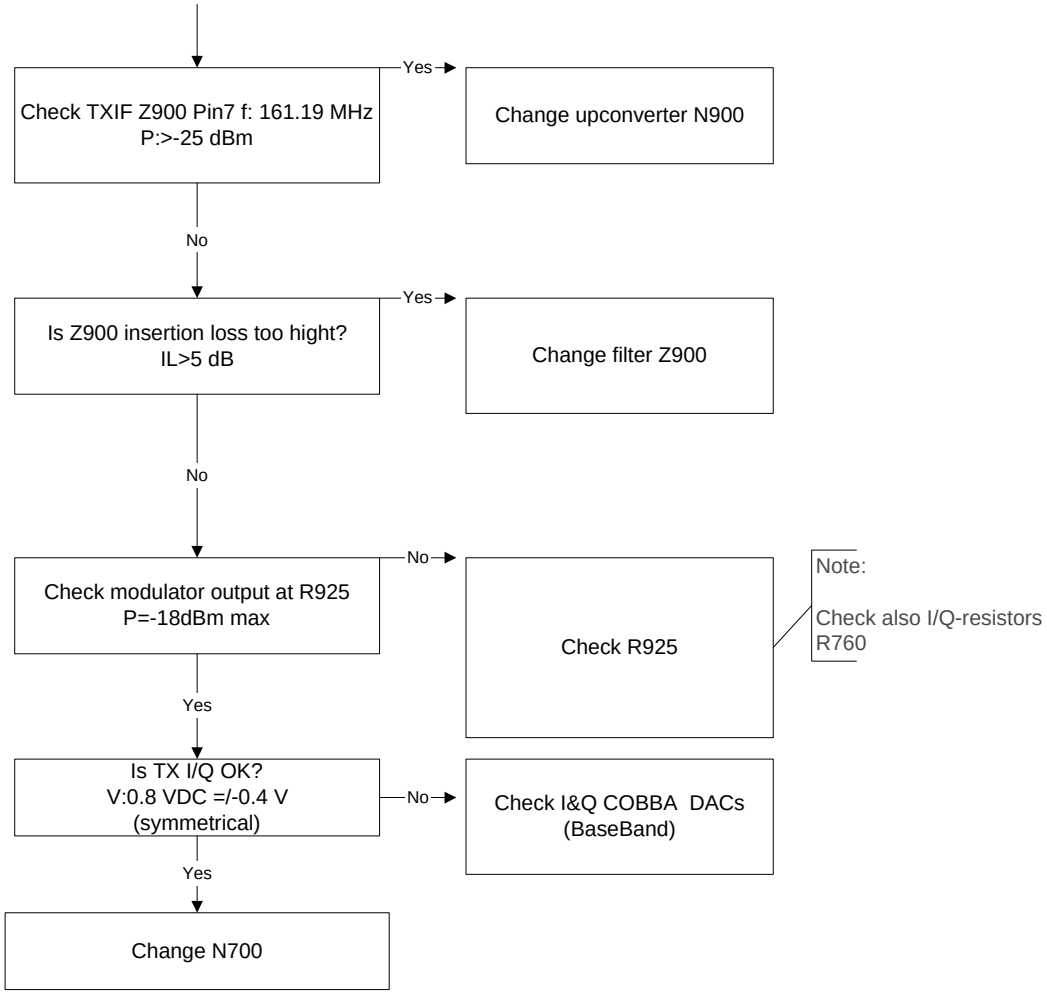
Power detection and power control circuits are located in the power control section of this manual.

Troubleshooting diagrams for TX

AMPS TX

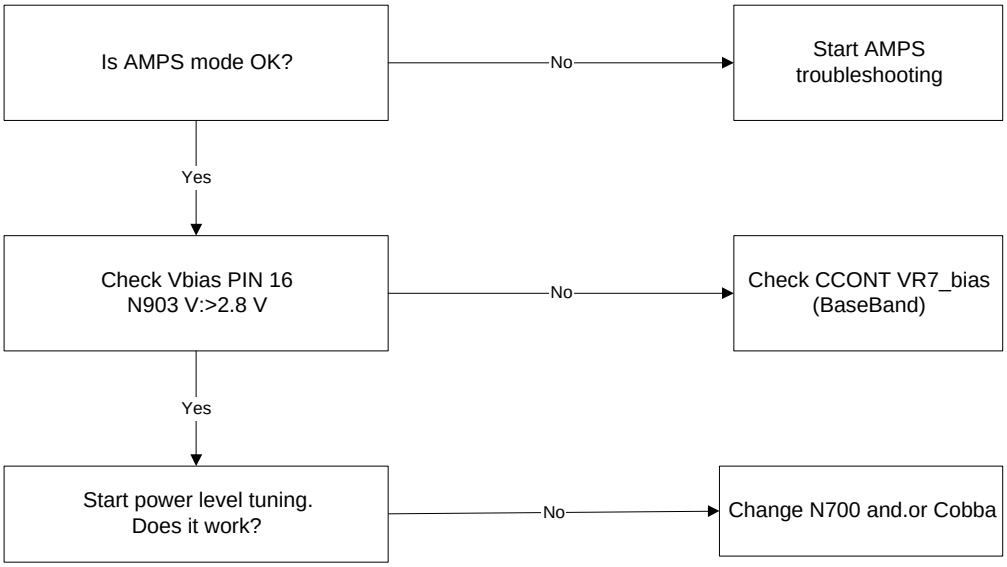
Connect an RF–cable to the antenna interface and connect the cable to a spectrum analyzer input. Start WinTesla software and set the phone to Analog mode. Set channel 383 and Powerlevel 2 and measure RF output level. Please notice insertion loss of the cable and attenuations in the test jig or antenna adapter. It is recommended to use an external attenuator to avoid overloading the spectrum analyzer.





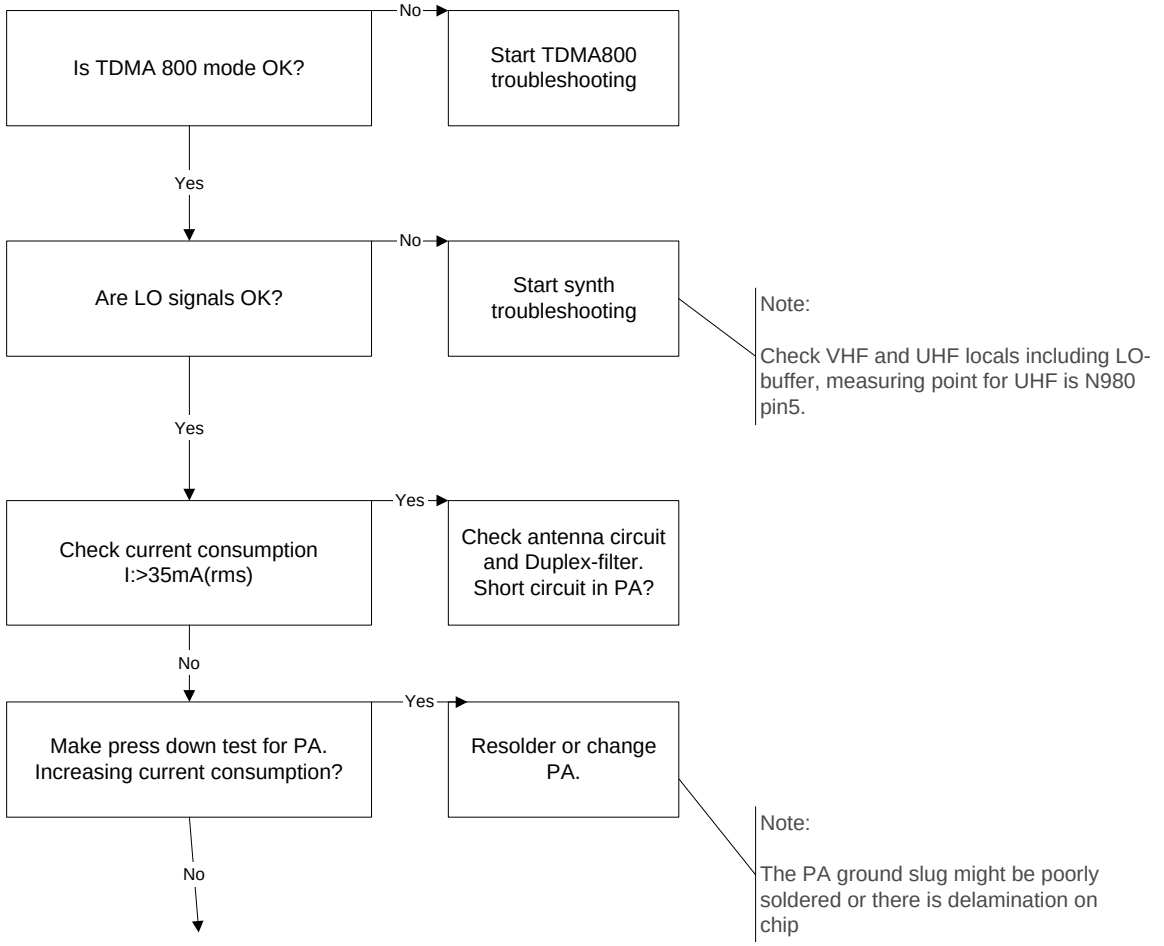
TDMA800 TX

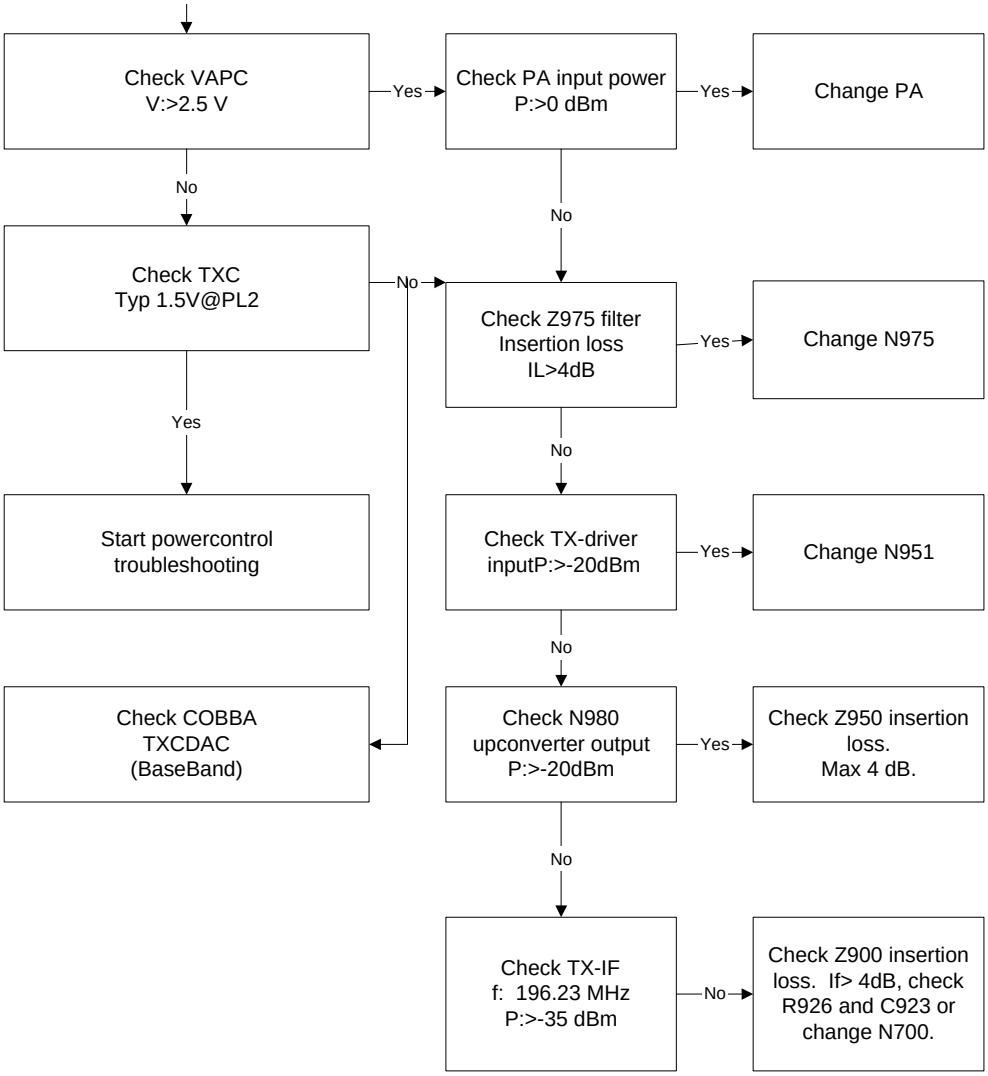
The transmitter chain is exactly the same as in AMPS mode, but the power amplifier is biased to more linear mode, so it is important that AMPS have no faults.



TDMA1900 TX

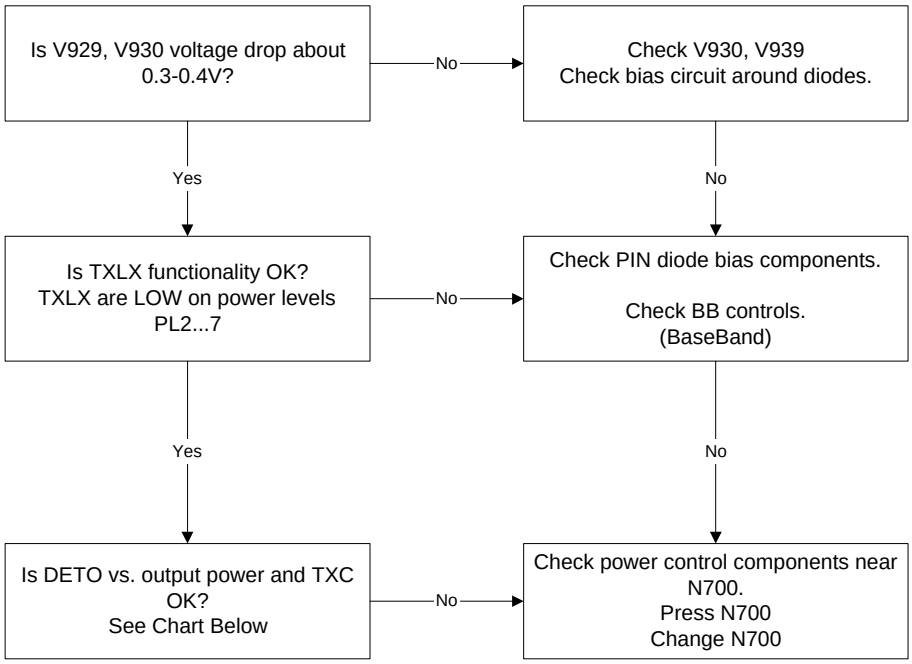
TDMA1900 mode and DAMPS mode have common IF section and antenna circuit and thus it is important that DAMPS mode have no faults.





Power control loop

Power control section is basically similar for both bands, except for that both bands have their own directional coupler and detector. The power control is actually made in the EROTUS IC.



800D					1900C			
	Pout	TXC	LB-DETO			Pout	TXC	UB-DETO
PL	dBm	dac	mV		PL	dBm	dac	mV
2	P26.8	250	1650		2	26.8	124	1478
3	23.5	77	1350		3	23.0	27	1275
4	20.0	-40	1120		4	20.0	-53	1120
5	16.0	-127	930		56	16.0	-128-	937
6	12.0	-187	840		6	12.0	177	831
7	8.0	-228	750		7	8.0	-215	762
8	4.0	-188	840		8	4.0	-205	768+
9	0.0	-229	740		9	0.0	-253	693
10	-4.0	-290	650		10	-4.0	-329	531

Synthesizers

There are four oscillators generating the needed frequencies for RF section: 19.44 MHz reference oscillator, 1GHz UHF VCO, 2Ghz UHF VCO, and VHF VCO. Only VHF VCO is discrete solution and it has two fixed frequencies (322.38 MHz for lowband and 392.46 MHz for upper band). VHF VCOs operating frequency is controlled by BAND–signal and the PLL circuit of EROTUS. All locals are locked to the stable reference oscillator.

The frequency range for 1GHz UHF VCO is 985.23 – 1010.2 MHz and for 2Ghz UHF VCO is 2046.2 – 2107.2 Mhz.

A practical way to check out synthesizer statusis to measure the control voltage of the VCO from the integrator capacitor C822 (LB) , C883 (HB), or C789 (VHF). The voltage must be stable and in the correct range, and the local oscillator is running correctly.

19.44 MHz Reference oscillator

The 19.44 MHz oscillator frequency (G850) is controlled by COBBA_D. This 19.44 MHz signal is connected to EROTUS and to the TDMA1900 PLL circuit.

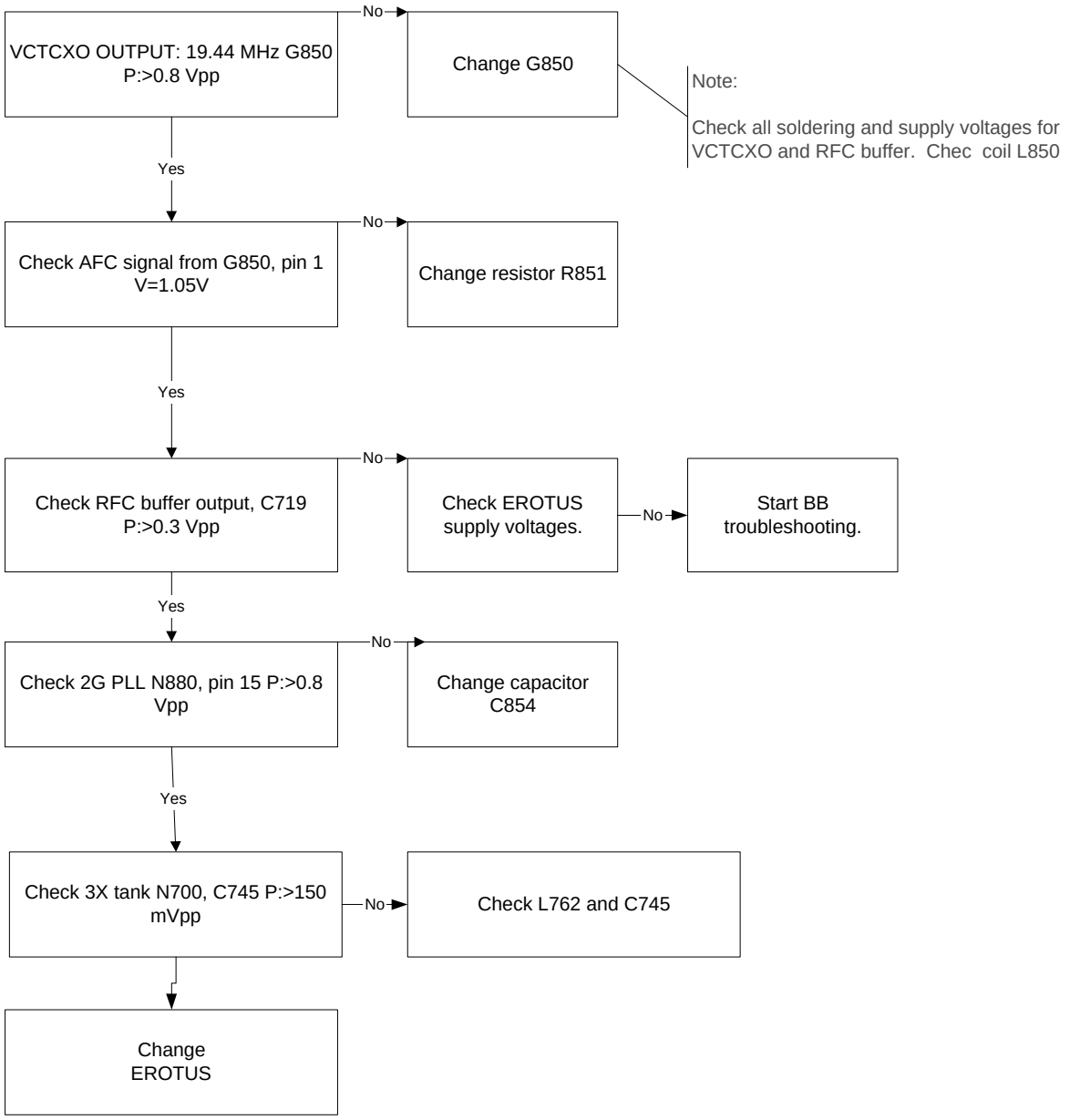
All synthesizers use the divided VCTCXO signal as reference signal for Phase locked loop to provide the correct LO frequency. The VCTCXO output signal is also used to generate multiple LO frequency by multipliers.

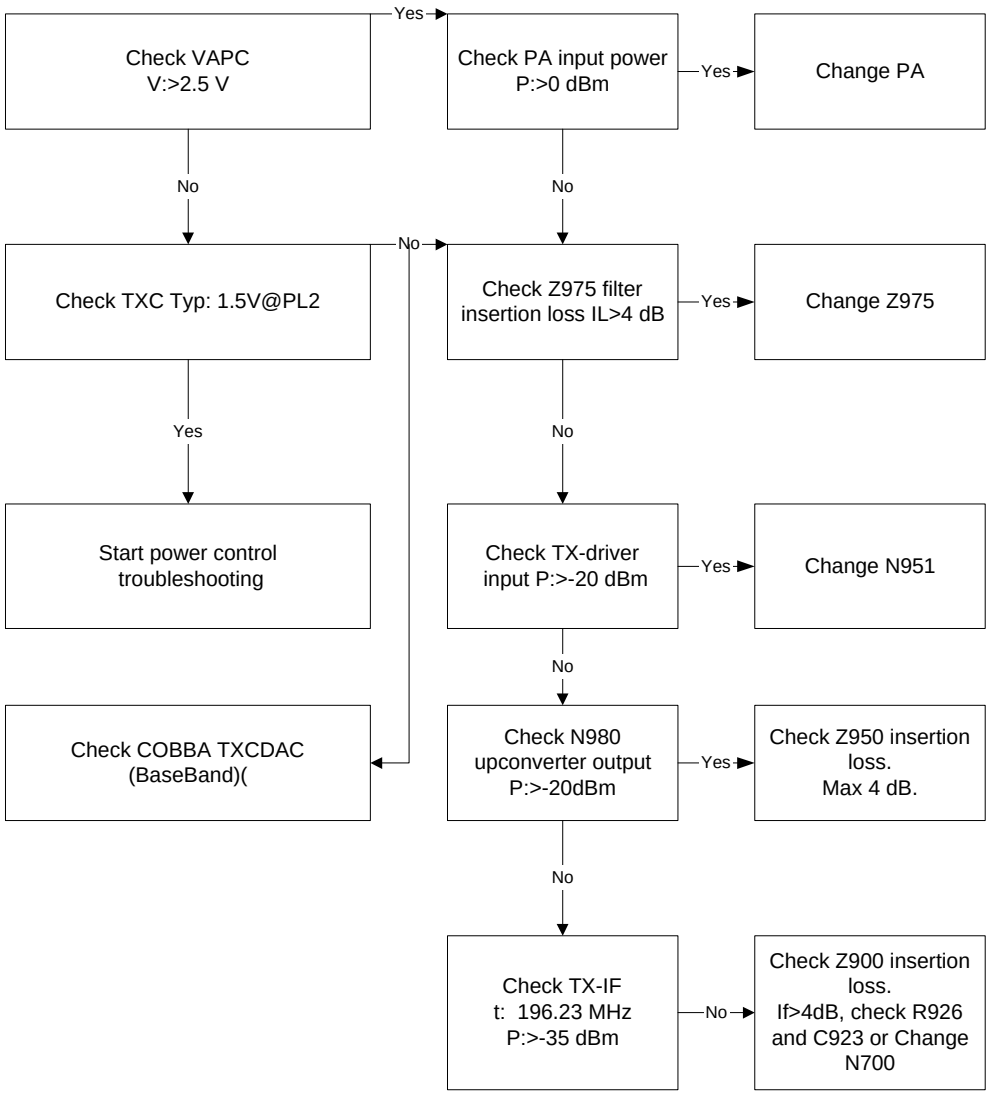
Baseband also needs the reference signal so it can generate necessary clock signals, and the VCTCXO output signal is also buffered and connected to MAD.

58.32 MHz Triple Multiplier

The 3–multiplier is a integrated solution in EROTUS and it is used to generate second LO frequency for the receivers. The 3*multiplier output signal is multiplied by 2 and then it is fed to the 2nd downconverter.

19.44 MHz oscillator

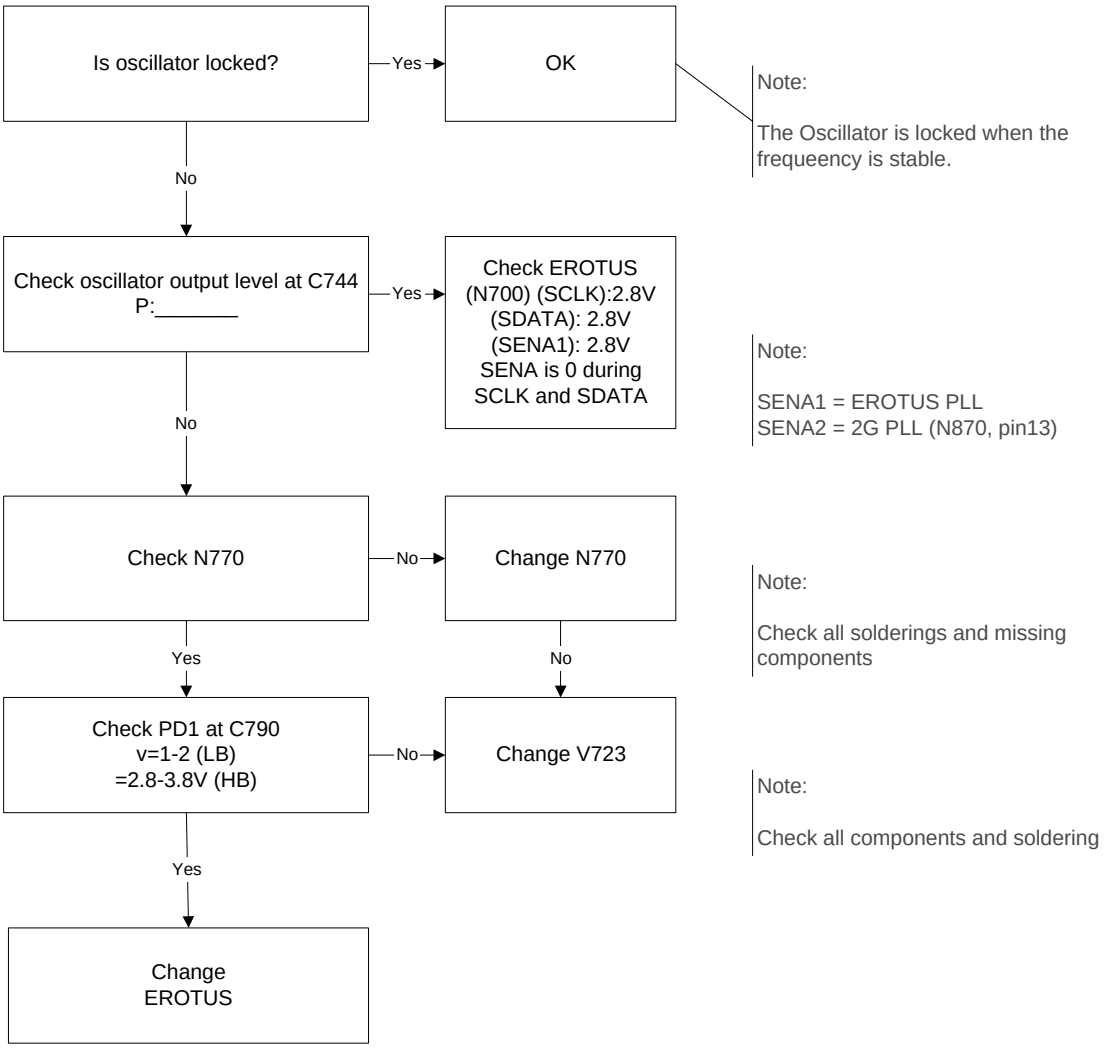




VHF VCO

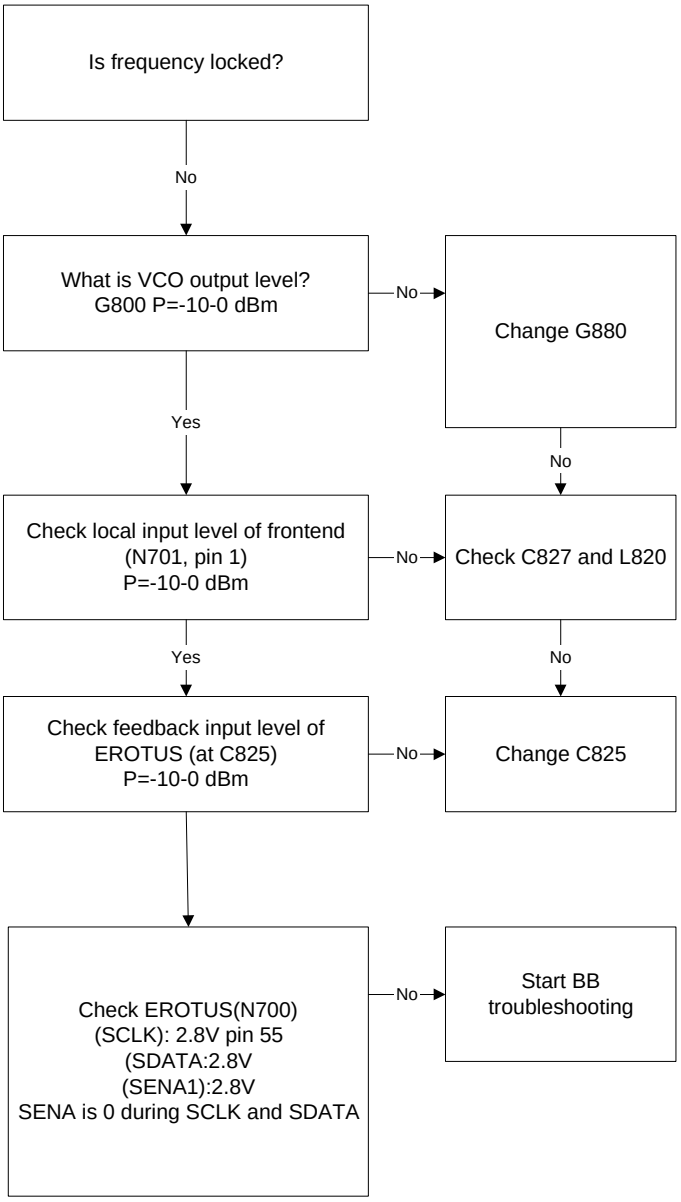
The VHF VCO signal is used to generate transmitter Intermediate frequencies. The VHF VCO has two fixed frequencies. Operating frequency is locked in Phase-locked Loop, which is controlled by baseband. Because the oscillator has two frequencies, it has also two different switching modes. These modes are controlled by a BAND–signal. In AMPS and TDMA800 modes, the VHF frequency is 322.38 MHz and logical level of BAND signal is “HIGH”. In TDMA1900 mode, a higher intermediate frequency is needed, so the operating frequency is increased to 392.46 MHz. The BAND signal is set to logical level “Zero”.

The VHF VCO output signal is fed to EROTUS LO–pin VV_in. Inside the EROTUS, the signal is divided for the Phase detector and TX parts. Before injection to the I/Q–modulator, the frequency is divided by 2 .


Is oscillator locked?
Yes
OK
Note:
The Oscillator is locked when the frequeency is stable.
No
Check oscillator output level at C744
P:_____
Yes
Check EROTUS
(N700) (SCLK):2.8V
(SDATA): 2.8V
(SENA1): 2.8V
SENA is 0 during
SCLK and SDATA
Note:
SENA1 = EROTUS PLL
SENA2 = 2G PLL (N870, pin13)
No
Check N770
No
Change N770
Note:
Check all solderings and missing components
Yes
No
Check PD1 at C790
v=1-2 (LB)
=2.8-3.8V (HB)
No
Change V723
Note:
Check all components and soldering
Yes
Change
EROTUS

AMPS and TDMA800 UHF Synthesizer

The 1 GHz UHF VCO (G880) generates the first injection for RX (869...897) and the final injection for TX (824...849 MHz). The output frequency of the module depends on the DC–control voltage supplied by EROTUS in line PD2.



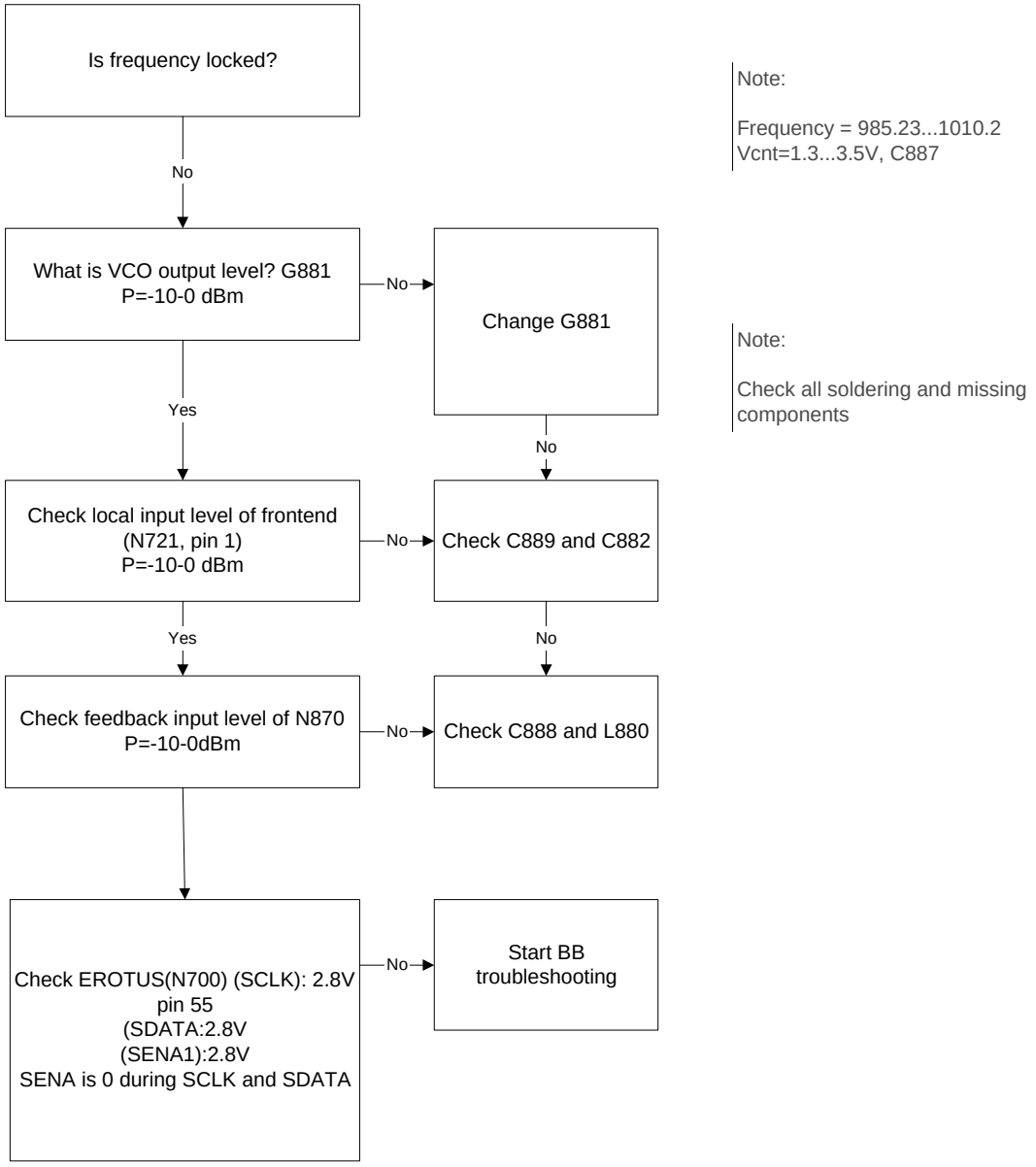
Note
Frequency = 985.23...1010.2
Vcnt=1.3...3.5V, C826

Note:

Check all soldering and missing components

TDMA1900 UHF Synthesizer

The 2GHz UHF synthesizer generates desired injection frequencies for TX and RX chain. The output frequency of the VCO depends on the control voltage of the PLL circuit.



RF ASIC Data

General Info

EROTUS (N700) provides three main RF functions:

1 RX/TX IF blocks

2 PLLs for VHF and 1 GHz UHF

3 TX Power control circuits

The receiver block consists of IF buffers, active mixers, 6 multiplier (3*+2*), AGC amplifier, and limiter.

The transmitter section includes a digital gain step amplifier, a linear gain control amplifier, a divider, an I/Q Modulator, and control part for the Transmitter Power Control loop.

The PLL section is controlled via the serial bus and contains both 1GHz UHF and VHF PLLs and prescalers.

EROTUS ASIC

Erotus is a uBGA–package, so RF probing for the most signals is impossible at EROTUS pins. Signals can be checked at those components, to which the signals are fed to.

Table 4: RX Front Ends N701 and N721

Pin No	Pin name	Nominal level	Description
1	LO IN	-5 dBm	Mixer LO input
2	Vdd buf	2.8 V	LO-buffer Vdd
3	LO out	0 dBm	LO-buffer output
4	GND	0	Ground
5	Vdd LNA	2.8 V	LNA Vdd
6	GND	0	Ground
7	LNA in	-	LNA RF input port
8	GND	0	LNA ground
9	Gain Sel	>2 V	LNA gain select
10	LNA out	-	LNA output port
11	GND	0	Ground
12	Mxr RF	-	Mixer RF input port
13	GND/1/2IF	0	Ground (1/2-IF tuning in N721)
14	MXR IF	-	Mixer IF input port
15	GND	0	Ground
16	Vdd MXR	2.8V	Mixer LO buffer Vdd and LO buffer tuning

Table 5: Power Amplifiers N903 and N960 — *RF9130 (N903)*

Pin No	Pin Name	Description
1	VCC	Power supply pin for bias circuit. Add RF bypass capacitor.

Table 5: Power Amplifiers N903 and N960 — *RF9130 (N903)*

Pin No	Pin Name	Description
2	L TUNE	Tuning pin for interstage matching network. A short **(TBD)???** transmission line length is required for tuning interstage match.
3	GND	Ground
4	VCC1	Power supply pin for the first stage collector. An RF choke and a bypass capacitor is required for this pin.
5	GND1	Ground pin for the first stage
6	RF IN	RF input, DC coupled
7	N/C	No connection or GND
8	V_{reg}	Regulated power supply for bias circuit. PA shutdown
9	GND	Ground
10	GND	Ground
11	GND	Ground
12	RF OUT	Same as pin 12
14	$2 * f_0$	Second harmonic trap. Add capacitor to ground
15	GND	Ground
16	V_{bias}	Bias control 2.8 V. Add RF bypass capacitor
Package base	Ground	Ground connection. The backside of the package should be connected to the ground plane through a short path

Table 6: Power Amplifiers N903 & N960 — *RF9131 (N960)*

Pin No	Pin Name	Description
1	N/C	No connection (GND)
2	VCC Q2C	Power supply pin for the 2nd stage. A bypass capacitor is required
3	N/C	No connection (GND)
4	VCC Q1C	Power supply pin for the 1st stage. A bypass capacitor is required.
5	N/C	No connection (GND)
6	RF IN	RF input. DC block on chip
7	N/C	No connection (GND)
8	VREG	Regulated voltage supply for the bias circuit
9	BIAS3	Bias ground

Pin No	Pin Name	Description
10	N/C	No connection (GND)
11	N/C	No connection (GND)
12	RF OUT	RF output. Use this pin for an output matching capacitor. **Do not feed bias through this pin** (DC coupled)
13	RF OUT	RF output and bias for the output stage. 3rd stage collector
14	RF OUT	RF output and bias for the output stage. 3rd stage collector
15	N/C	No connection (GND)
16	N/C	No connection (GND)
Package base	Ground	Ground connection. The backside of the package should be connected to the ground plane through a short path.

Table 7: PENTA Regulator N702

Pin No	Pin name	Nominal level	Description
1	Bypass	-	Pin for external bypass capacitor
2	Common enable	>2 V	Enable for the whole circuit
3	VR1 cntrl	>2 V	Regulator 1 ON/OFF
4	VR2 cntrl	>2 V	Regulator 2 ON/OFF
5	VR3 cntrl	>2 V	Regulator 3 ON/OFF
6	VR4 cntrl	>2 V	Regulator 4 ON/OFF
7	VR5 cntrl	>2 V	Regulator 5 ON/OFF
8	GND	0	Ground
9	VR5	2.8 V	Regulator 5 output
10	Vcc2	VBAT	VR4 and VR5 common input voltage
11	VR4	2.8 V	Regulator 4 output
12	VR3	2.8 V	Regulator 3 output
13	VR2	2.8 V	Regulator 2 output
14	VR1	2.8 V	Regulator 1 output
15	Vcc1	VBAT	VR1, VR2, and VR3 common input voltage
16	N/C		Not connected

Table 8: TDMA 1900 Upconverter N980

Pin No	Pin name	Nominal level	Description
1	VDD1	2.8 V	Supply voltage
2	N/C		Not connected
3	N/C		Not connected
4	GND	0	Ground
5	LO IN	0 dBm	TX local input
6	GND	0	Ground
7	RF OUT	-	RF output
8	VDD2	2.8 V	Supply voltage
9	N/C		Not connected
10	N/C		Not connected
11	GND	0	Ground
12	VDD3	2.8 V	Supply voltage
13	GND	0	Ground
14	IF IN	-	Intermediate frequency input
15	N/C		Not connected
16	TX ENA	>2 V	TX enable

Table 9: TDMA 1900 PLL Circuit N870

Pin No	Pin name	Nominal level	Description
1	FAST	2.8 V	Enable input for fast charge pump
2	CPF	-	Fast charge pump output
3	CP	-	Normal charge pump output
4	VDD2	2.8 V	Power supply voltage
5	Vss3	0	Ground
6	RFI	-	Main divider input
7	Vss2	0	Ground
8	POL	2.8 V	Polarity select
9	PON	2.8 V	Power on input
10	Vss1	0	Ground
11	CLK	2.8 V	Programming bus clock input
12	DATA	2.8 V	Programming bus data input

Pin No	Pin name	Nominal level	Description
13	E	2.8 V	Programming bus enable input
14	Vdd1	2.8 V	Power supply voltage
15	XTALB	-	Complementary crystal frequency input
16	XTALA	-	Complementary crystal frequency input
17	GND (CP)	0	Ground for charge pump
18	Vcc	4.8 V	Supply voltage for charge pump
19	Iset	-	Charge pumpt currents setting
20	LOCK	-	Out of lock detector